



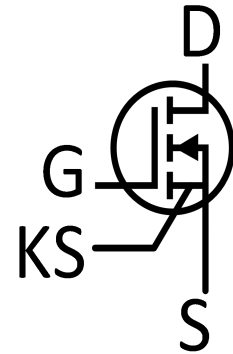
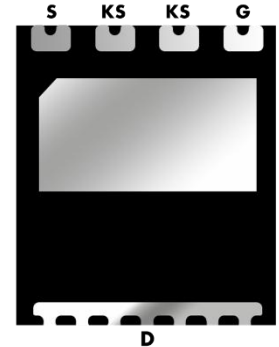
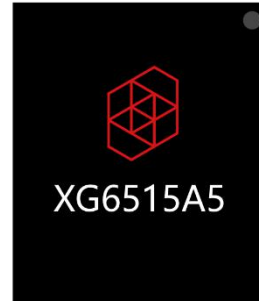
XG6515A5

650V 150mΩ E-Mode GaN HEMT

Features

BV_{dss}	R_{dson}	I_{ds}
650V	150mΩ	8A

- Ultra-low $R_{ds(on)}$
- High dv/dt capability
- Extremely low input capacitance
- Zero Q_{rr}
- Outstanding switching performance
- Low System Profile
- Single Gate Pin



Application

- Switching Power Supplies
- PC and Server Power Supplies
- Adapters, Quick Chargers
- 5G Power Supplies

Description

- These devices are N-channel 650 V Power GaN HEMTs based on proprietary E-mode GaN-on-silicon technology. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge, making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.

Type	Package	Qty
XD6515A5	DFN5*6	2500

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650V E-Mode GaN

Device Characteristics

Static Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$ $I_d=3.5mA$	0.7	1.0	1.3	V
2	BV_{dss}	Drain-Source breakdown voltage	$V_{gs}=0V$ $I_d=25\mu A$	650			V
3	I_{dss}	Zero gate voltage drain current, $T_C = 25^\circ C$	$V_{gs}=0V$ $V_{ds}=650V$		3		μA
4	I_{dss}	Zero gate voltage drain current, $T_C = 150^\circ C$	$V_{gs}=0V$ $V_{ds}=650V$		18		μA
5	I_{gss}	Gate-Source Leakage	$V_{gs} = 6V$ $V_{ds} = 0V$		30		μA
6	R_{dson}	Static drain-source on resistance, $T_C = 25^\circ C$	$V_{gs}=6V$ $I_d=5A T_j=25^\circ C$		148		m Ω
			$V_{gs}=6V$ $I_d=5A T_j=150^\circ C$		310		
7	V_{sd}	Reverse conduction voltage	$I_{sd}=1A$ $V_{gs}=0V$	1.6	1.8	2.1	V
Dynamic Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	C_{iss}	Input capacitance	$V_{gs}=0V$ $V_{ds}=400V$ $f=1MHz$		78		pf
	C_{oss}	Output capacitance			33		pf
	C_{riss}	Reverse transfer capacitance			0.3		pf
2	Q_g	Gate charge	$V_{ds}=400V$ $I_d=6A$ $V_{gs}=6V$		2.5		nC
	Q_{gs}	Gate to source charge			1		nC
	Q_{gd}	Gate to drain charge			0.8		nC
3	Q_{rr}	Reverse recovery charge			0		nC
Switching Performance				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	$t_{d(on)}$	Turn-on delay time	$V_{ds}=400V$ $I_d=2.5A$ $R_g=10\Omega$ $V_{gs}=6V$		3		ns
2	t_r	Rise time			13		ns
3	$t_{d(off)}$	Turn-off delay time			7		ns
4	t_f	Fall time			16		ns

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Absolute **Max.** Ratings

	Symbols	Parameters	Value	Unit
1	V_{DS-max}	Breakdown voltage transient @ $T_{case}=25^{\circ}C$	750	V
2	V_{GS-max}	Gate to source max. transient voltage @ $T_{case}=25^{\circ}C$	-15 to +7	V
3	I_{ds-max}	Drain to source DC current @ $T_{case}=25^{\circ}C$	8	A
4	I_{ds-max}	Drain to source DC current @ $T_{case}=100^{\circ}C$	6	A
5	$dv/dt-max$	Drain to source voltage slew rate	150	V/nS
6	T_{J-max}	Max junction temperature	150	$^{\circ}C$
7	$T_{S-storage}$	Storage temperature	-55 to 150	$^{\circ}C$

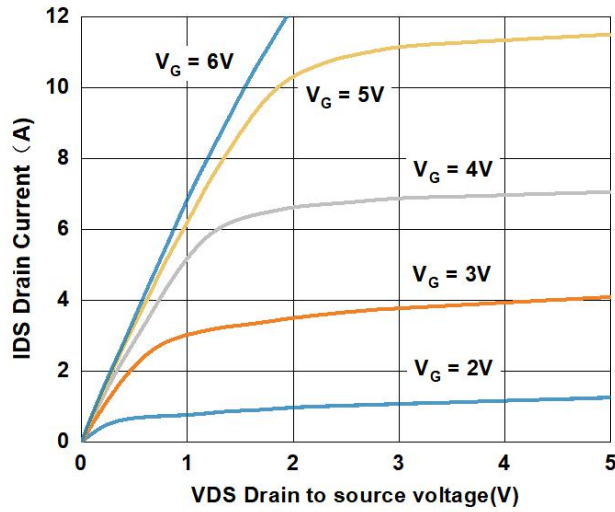
Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	1.67	$^{\circ}C /W$
2	R_{thJA}	Thermal resistance (junction to ambient)	60	$^{\circ}C /W$
3	T_{solder}	Reflow soldering temperature	250	$^{\circ}C$

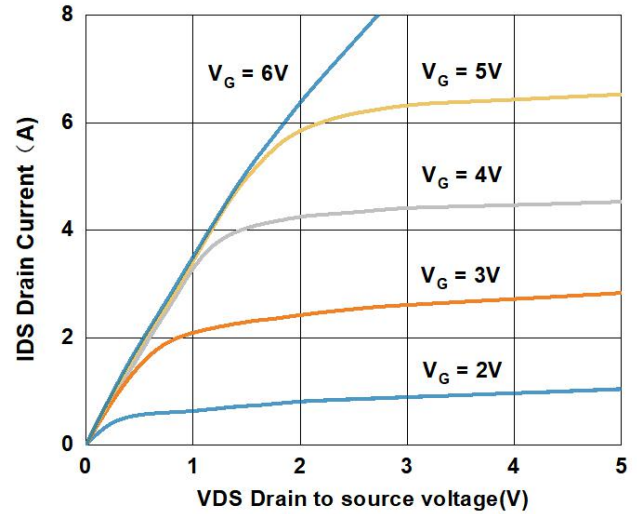
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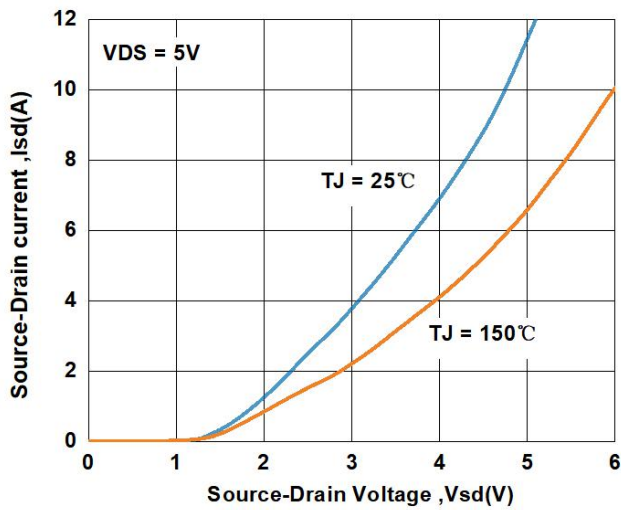
Electrical Performance



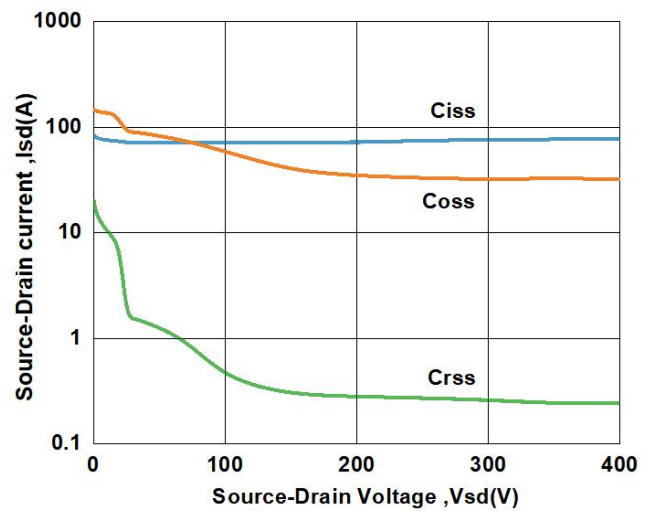
$I_{ds} - V_{ds}$ curves @25 °C



$I_{ds} - V_{ds}$ curves @150 °C



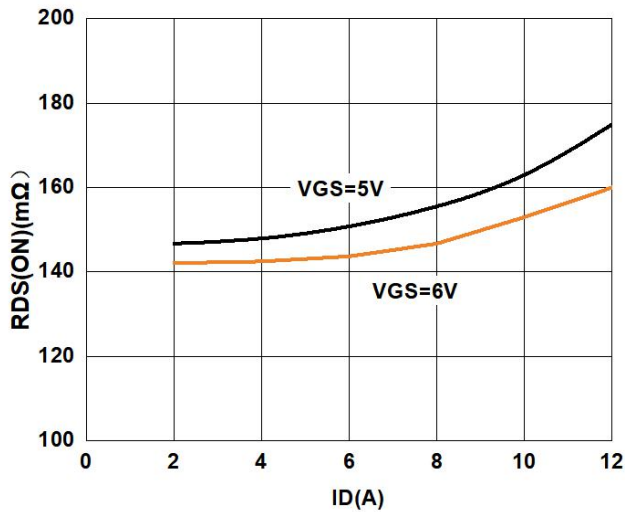
Transfer curves @25 °C & 150 °C



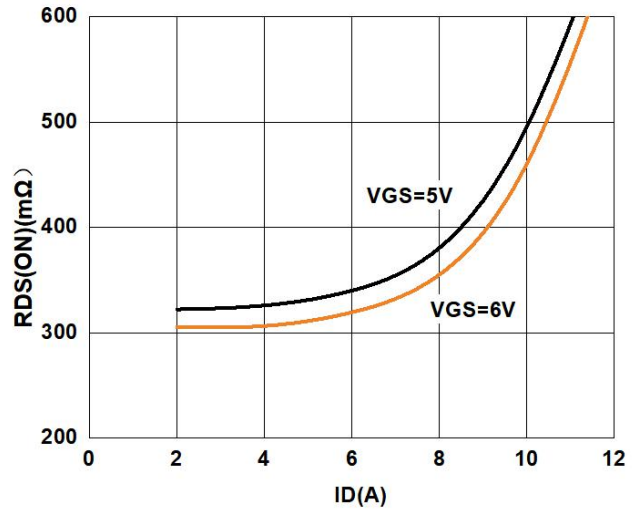
Capacitance curves

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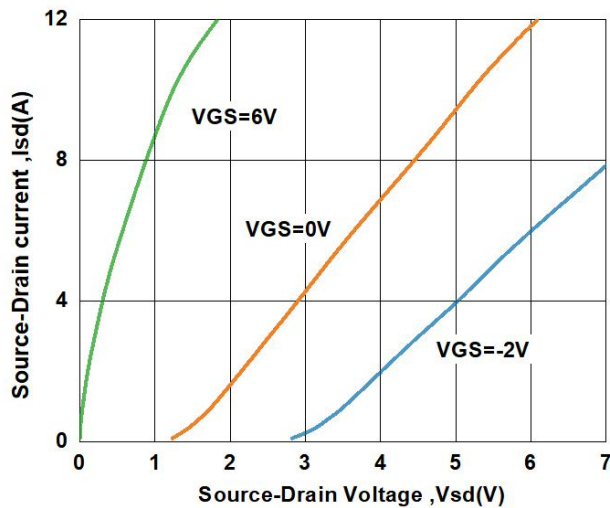
650V E-Mode GaN



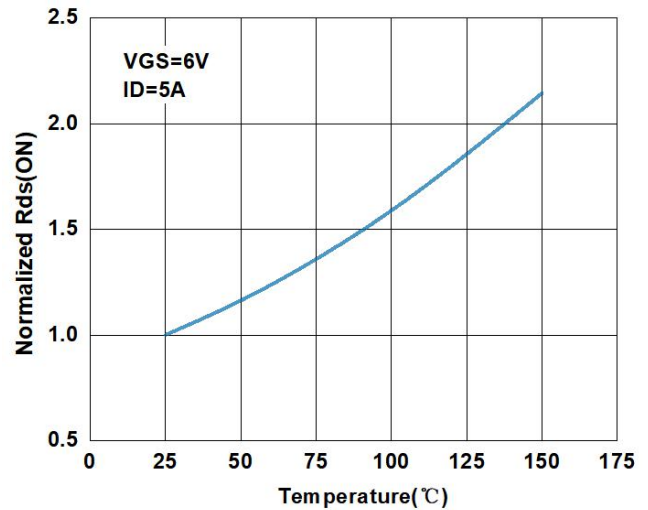
ON-resistance for various drain current @T_j=25°C



ON-resistance for various drain current @T_j=150°C



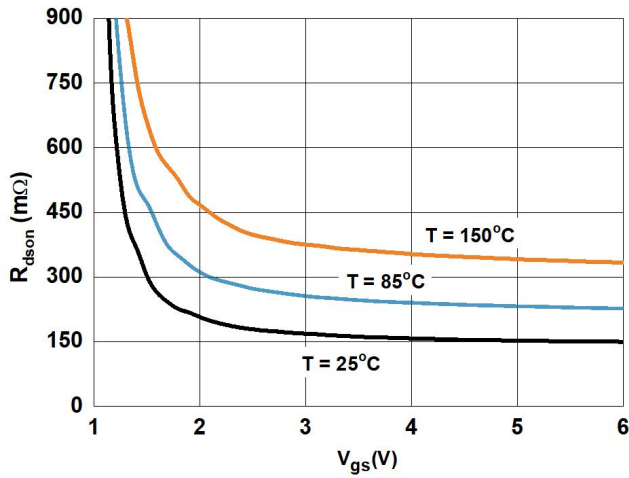
Reverse conducting curves



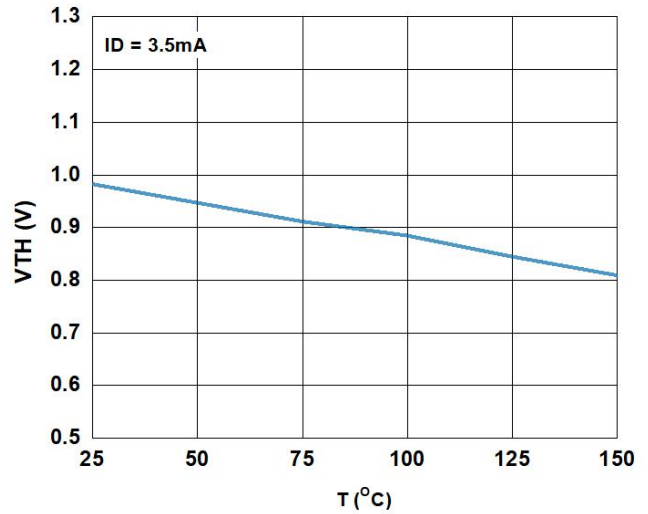
ON-resistance @ different temperatures

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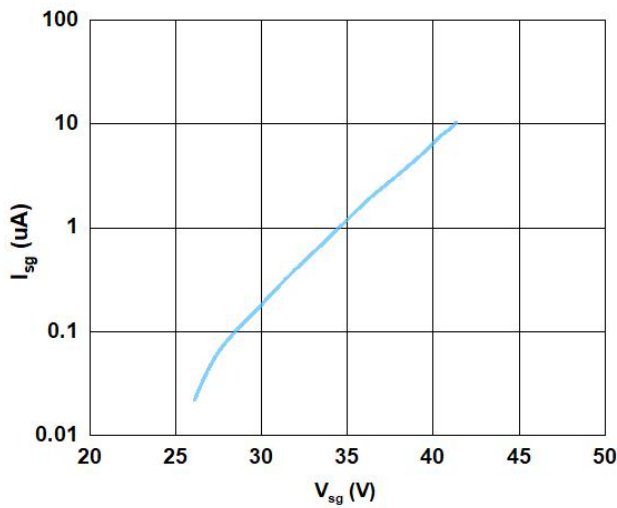
650V E-Mode GaN



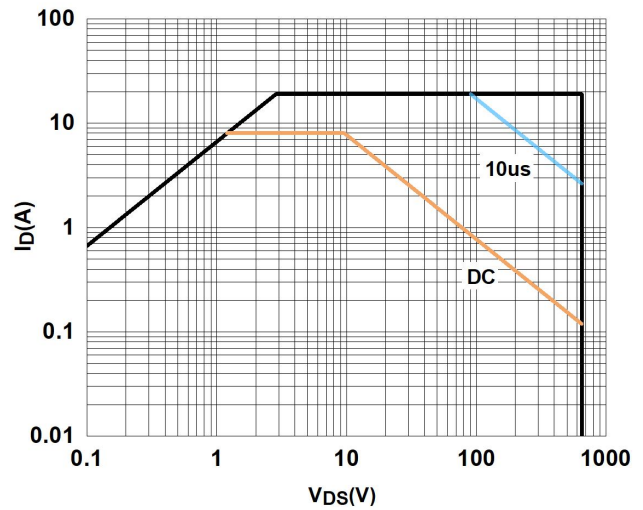
ON-resistance for @ different V_{gs}
@T=25°C & 85°C & 150°C



V_{th} @ different temperatures



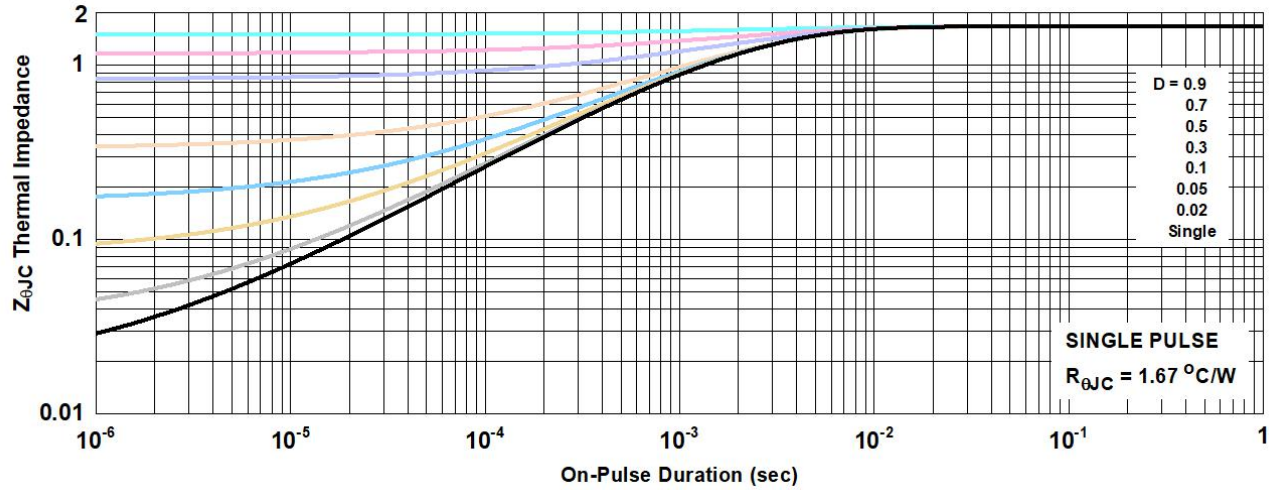
Reverse Gate Voltage



Safe Operation Area

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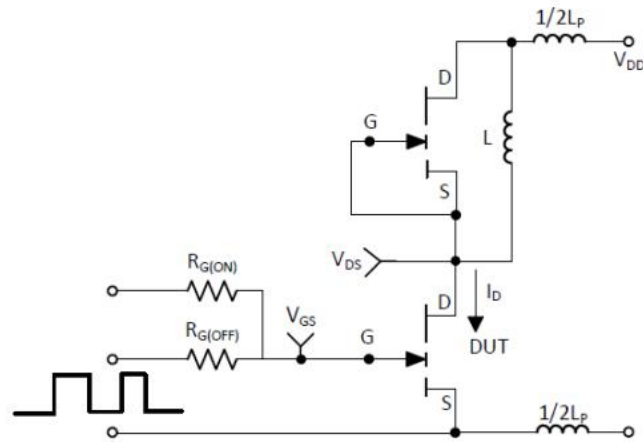
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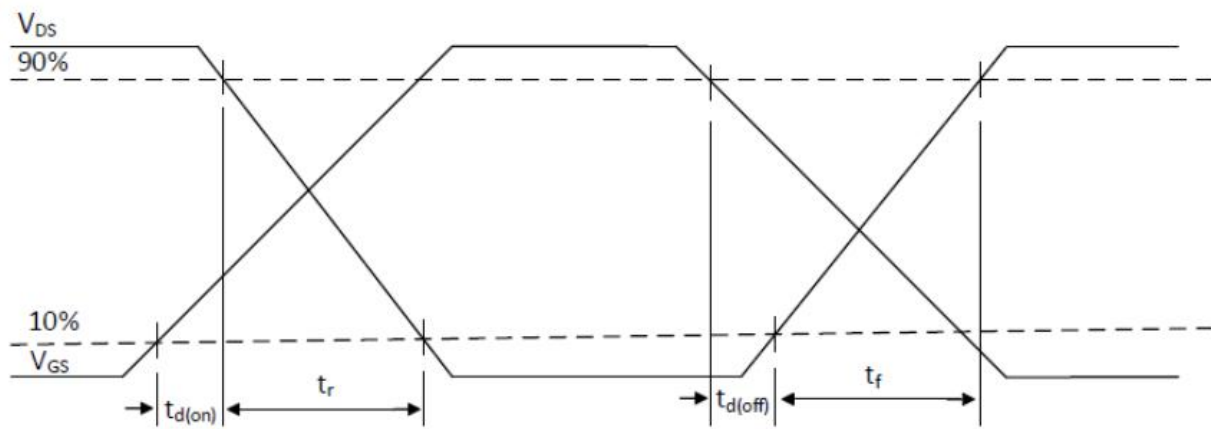
Transient Thermal Impedance

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Switching Test Circuit

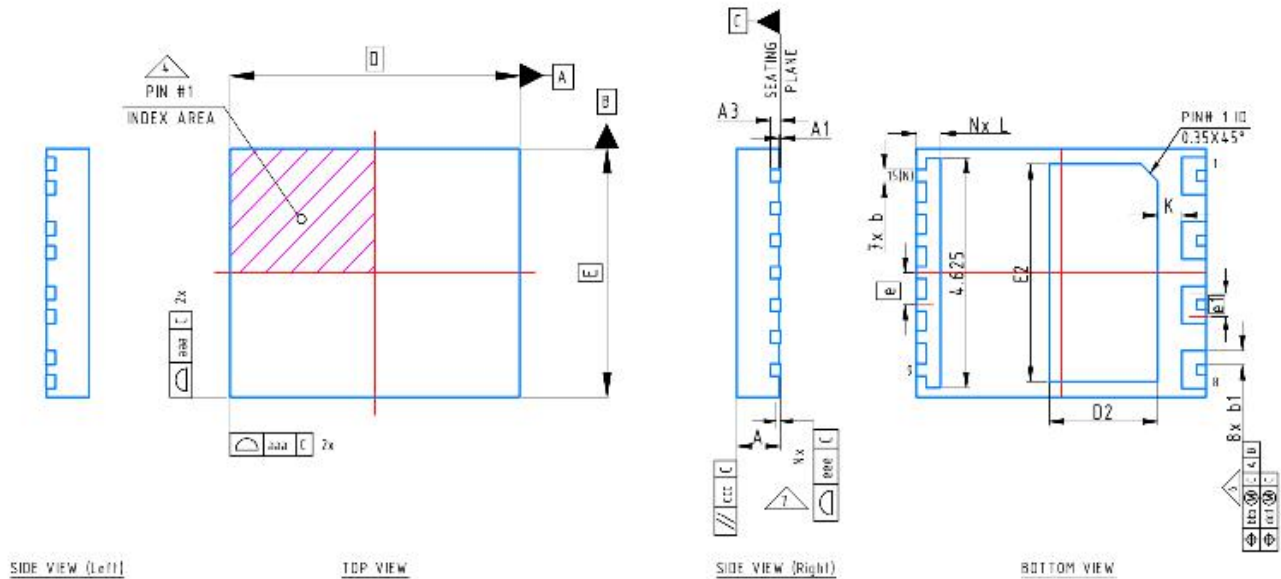


Switching Time Waveform

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Package Information



Thickness Symbol	V			W			NOTE
	MINIMUM	NOMINAL	MAXIMUM	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	0.70	0.75	0.80	
A1	0.00	0.02	0.05	0.00	0.02	0.05	
A3	---	0.203 Ref	---	---	0.203 Ref	---	
b	0.200	0.250	0.300	0.200	0.250	0.300	6
b1	0.225	0.275	0.325	0.225	0.275	0.325	6
D	6.000 BSC			6.000 BSC			
E	5.000 BSC			5.000 BSC			
e	0.650 BSC			0.650 BSC			
e1	0.475 BSC			0.475 BSC			
E2	2.250	2.250	2.350	2.150	2.250	2.350	
E2	4.270	4.370	4.470	4.270	4.370	4.470	
K	0.20	---	---	0.20	---	---	
L	0.400	0.500	0.600	0.400	0.500	0.600	
aaa	0.05			0.05			
bbb	0.10			0.10			
ccc	0.10			0.10			
ddd	0.05			0.05			
eee	0.08			0.08			
N	15			3			
NE	8/7			5			
NOTES	1, 2						
LF PART NO.	445811/446251						

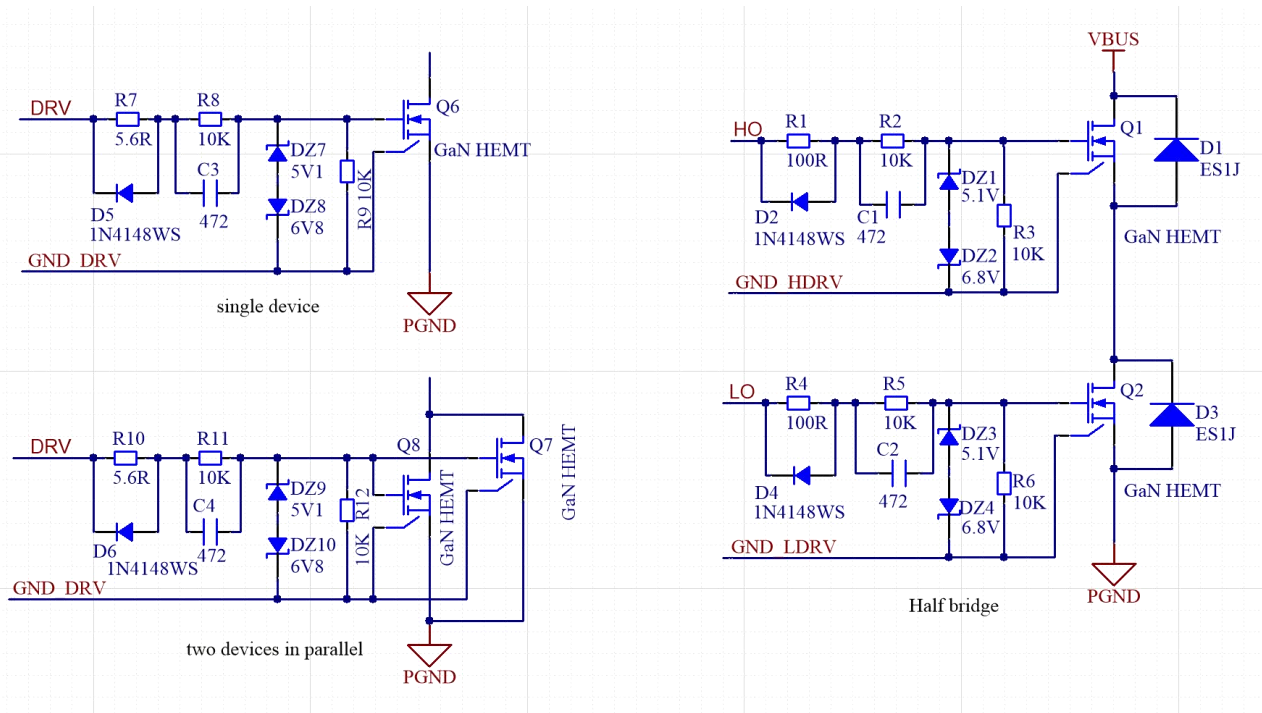
NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. NE refers to the maximum number of terminals E side.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

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Gate Driving Examples



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Revision History

Revision History



Document revision	Date	Description of changes
2.7	2023.10.11	Target datasheet

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